A 250 mV 7.5 μW 61 dB SNDR SC ΔΣ Modulator Using Near-Threshold-Voltage-Biased Inverter Amplifiers in 130 nm CMOS

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***Abstract*—An ultra-low voltage switched-capacitor (SC) ΔΣ converter running at a record low supply voltage of only 250 mV is introduced. System level aspects are discussed and special circuit techniques described, that enable robust operation at such a low supply voltage. Using a SC biasing approach, inverter-based integrators are realized with overdrives close to the transistor threshold voltage $V_{\rm th}$ while compensating for process, voltage and temperature (PVT) variation. Biasing voltages are generated on-chip using a novel level shifting circuit, that overcomes headroom limitations due to saturation voltage $V_{\rm sat}$. With an oversampling ratio (OSR) of 70 and a sampling frequency (f_S) of 1.4 MHz at 250 mV power supply the converter achieves 61 dB SNDR in 10 kHz bandwidth while consuming a total power of 7.5 μW.**

***Index Terms*—Analog integrated circuits, analog-to-digital converter, delta-sigma, inverter-based switched capacitor circuits, low power, ultra-low voltage.**

I. Introduction

WHEREAS in the past years high-performance circuits were of main interest, a new trend towards extremely low power and ultra-low voltage circuit techniques [1]–[9] is emerging. This is motivated by technology scaling as well as biomedical [10], [11] and energy scavenging applications [12]–[14].

A consequence of device shrinking is a continuously decreasing supply voltage, which cannot be easily compensated by equal reduction in $V_{\rm th}$ due to leakage current. However, larger $V_{\rm th}$ relative to the supply voltage results in reduced current drive in analog circuits. Moreover, the speed and area advantage of deeply scaled nanometer technologies is traded against analog device characteristics like intrinsic gain and device variability. Consequently, analog circuit design in a digitally optimized technology is a challenging task, that needs to maintain functionality, robustness and performance with inferior analog device parameters at a lower supply voltage.

Apart from those technology constraints, low voltage and low power is dictated by biomedical compatibility requirements, for human body potentials are in the order of magnitude of 100 mV and excessive device heating must be avoided in sensitive body regions like the human brain. Recent works report on biomedical interfaces running on a supply voltage down to 0.5 V [11].

Finally, there exist numerous energy sources that can only provide power at a low voltage level. Inductive and thermoelectric energy harvesters [14] fall into this category as well as solutions that derive their power from natural energy sources like tree potentials [15]. These energy scavengers are highly attractive for portable devices and applications that are not easily accessible for regular battery replacement (human body and wireless sensor nodes). However, in order to make these novel technologies available for the application, either the output voltage level has to be boosted or the circuitry has to be adapted for ultra-low voltage capability. Voltage boosting comes with the advantage of compatibility to standard circuits but efficient charge pumping under current loading conditions is extremely difficult at supply voltages below 300 mV due to the small on-off voltage difference and the large $V_{\rm th}$ relative to the supply voltage. Although boosters with 35 mV [12] and 95 mV [16] start-up voltages were proposed, these topologies rely either on mechanical start-up elements [12] or device programming [16] which depending on the application might raise long term reliability issues. Therefore, intrinsic ultra-low voltage techniques are proposed and demonstrated on a 250 mV ΔΣ converter in this work, thereby making direct powering possible and eliminating the need of voltage boosters for power generation. Although ultra-low voltage ΔΣ converters have already been proposed [1], [17]–[21], the lowest reported supply voltage is 0.5 V. Thus, this work sets a new state-of-the-art value by operating at only 250 mV.

The paper is organized as follows. Section II introduces the challenges in ultra-low voltage circuit design. In Section III the system level architecture of the proposed ΔΣ converter is discussed and Section IV describes the circuit design for the converter. Finally, measurement results are presented in Section V and Section VI ends with a conclusion.

II. Ultra-Low Voltage Design Challenges

The direct consequence of lowering the supply voltage is limited overdrive and voltage headroom. Thus, achieving sufficient performance while maintaining large common mode rejection ratio (CMRR) and robust operation over PVT variation is a key challenge. The minimum possible supply voltage $V_{\rm DD}$ and input common mode (CM) voltage $V_{\rm in_{CM}}$ for a certain process

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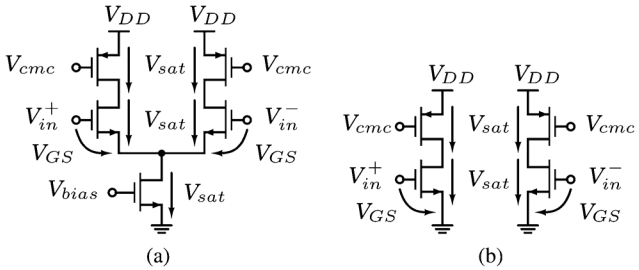


Fig. 1. Voltage drops in differential input pairs. (a) With tail current source. (b) Without tail current source.

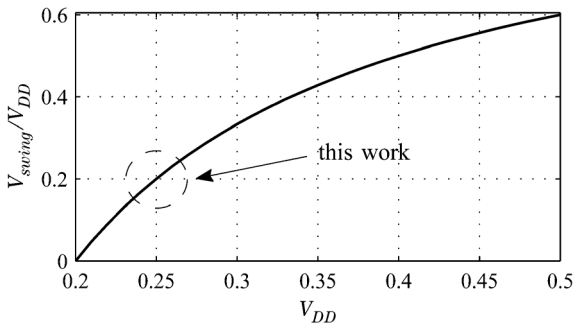


Fig. 2. Relative voltage swing versus supply voltage.

variation $\Delta V_{\rm th}$ can be derived for the classical differential pair [Fig. 1(a)] as

$$V_{\rm DD} \geq 3 \cdot V_{\rm sat} + |\Delta V_{\rm th}| \quad (1)$$

$$V_{\rm in_{CM}} \geq V_{\rm sat} + |\Delta V_{\rm th}| + V_{\rm GS} = V_{\rm sat} + |\Delta V_{\rm th}| + V_{\rm th} + V_{\rm ov} \quad (2)$$

with saturation voltage $V_{\rm sat}$ and overdrive $V_{\rm ov}$. Assuming subthreshold operation with $V_{\rm sat} \approx 90$ mV, $V_{\rm th} = 0.25$ V, $\Delta V_{\rm th} = 0.2 \cdot V_{\rm th} = 50$ mV and $V_{\rm ov} = -50$ mV this yields $V_{\rm DD} \geq 0.32$ V and $V_{\rm in_{CM}} \geq 0.34$ V. As a result, the minimum supply voltage is limited by $V_{\rm sat}$ and $|\Delta V_{\rm th}|$, whereas the input CM range and overdrive are mainly limited by $V_{\rm th}$.

In (1) it is assumed that the input CM is constant. By adjusting the input CM according to the $V_{\rm th}$ variation the term $\Delta V_{\rm th}$ can be eliminated, thus reducing the minimum power supply. On the other hand, large input CM swings will require additional headroom, leading to an increase in supply voltage.

To enable operation below 0.34 V, the tail current source must be omitted [Fig. 1(b)] [13], [22]. In this case the minimum supply voltage is decreased to $2 \cdot V_{\rm sat} \approx 180$ mV with the penalty of loss in CMRR.

For inverter based amplifiers [1] and output stages an additional limitation appears, namely the output swing $V_{\rm swing}$. This restricts the supply voltage to

$$V_{\rm DD} \geq 2 \cdot V_{\rm sat} + V_{\rm swing}. \quad (3)$$

Therefore, the minimum supply voltage is actually dictated by the minimum swing that the analog circuit can still operate with. The available voltage swing relative to the supply decreases nonlinearly (Fig. 2) and approaches zero at $V_{\rm DD} = 2 \cdot V_{\rm sat}$, the hard limit for analog circuits.

To conclude, whereas for $V_{\rm DD} \geq 0.5$ V the limiting factor is $V_{\rm th}$, for supply voltages below 0.5 V the major break in performance is caused by $V_{\rm sat}$, which unfortunately does not scale with technology.

In order to break the $V_{\rm sat}$ limitation and enable operation below 250 mV, time domain solutions can be employed. A highly efficient converter with 82 fJ per conversion and an SNDR of 60.3 dB running at 200 mV supply voltage has been proposed [23]. While a $\Delta\Sigma$ converter achieves noise shaping via feedback, that modulator is based on $\Delta\Sigma$ equivalent open loop noise shaping, which enables the use of a time domain integrator. As the signal is integrated in the time domain it is not subjected to voltage noise and the circuit design only needs to rely on digitally operated inverters, that can run below 200 mV. Consequently, time domain solutions overcome the $V_{\rm DS}$ restriction of traditional voltage domain solutions and are therefore well suited for deeply scaled technologies at very low supply voltages. However, the time domain converter [23] is restricted to open loop operation, so that high intrinsic linearity of the VCO is required, which is a major challenge in this design.

III. System Level Architecture

The system level design incorporates the definition of an appropriate ultra-low voltage loop topology as well as adjusting the coefficients, OSR and scaling coefficients for optimum performance at $V_{\rm DD} = 250$ mV.

A. Loop Topology

As pointed out in Section II limited voltage swing and CMRR are the major obstacles in realizing ultra-low voltage analog circuits. This translates into the requirement of a low-swing loop topology with CM cancellation.

Feedback topologies provide higher order integrated low-pass filtering but the integrators in the loop need to process the signal. This requires large integrator voltage swings. In contrast, the feedforward structure with input coupling allows the integrators to process the error signal only, thereby reducing the integrator voltage swings significantly [24].

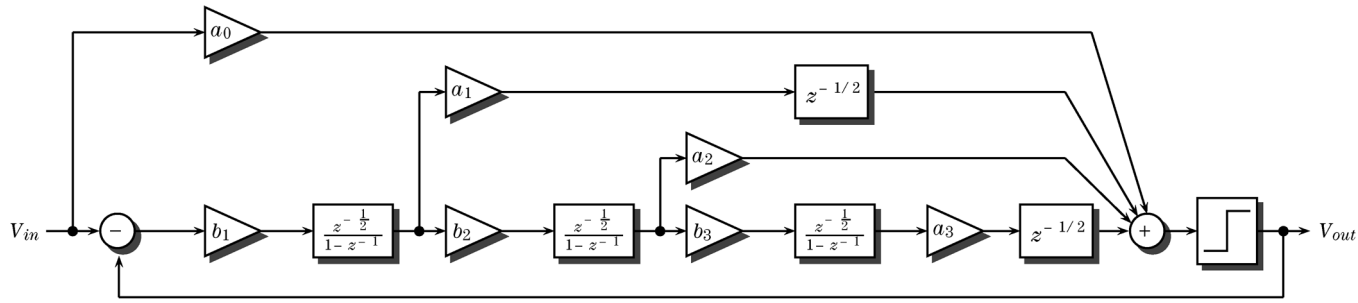
As SC techniques provide capacitive biasing, offset compensation and efficient CM cancellation (Section IV), a discrete time (DT) realization is preferred to a continuous time (CT) one.

Moreover, since simplicity is beneficial for ultra-low voltage design, a single-loop structure with single-bit quantization was adopted.

Therefore, a DT feedforward structure is the most convenient way to implement data converters down to 250 mV power supply. The feedforward loop structure is shown for third order in Fig. 3. As will be explained later in Section IV-B, the low voltage circuit implementation requires a calibration phase before each integration step. On the system level, this results in the half delay integrators [1] shown in Fig. 3.

B. Order and Oversampling Ratio

In order to analyze the dependence of SNDR on loop order and OSR, the converter was modeled in Matlab/Simulink up to



a_0	a_1	a_2	a_3	b_1	b_2	b_3
0.8	5.5	1.7	0.8	1/8	1	1/3

Fig. 3. Feedforward structure with input coupling.

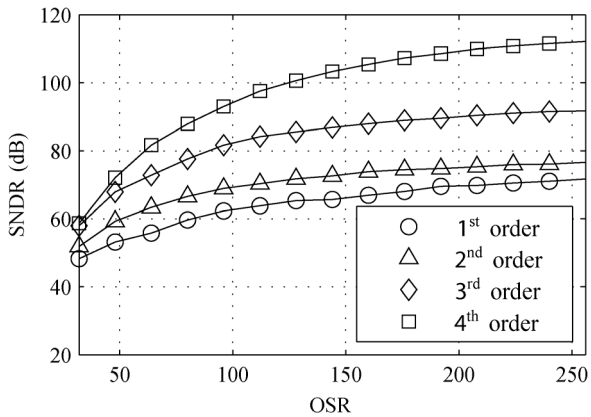


Fig. 4. SNDR versus OSR for finite opamp gain $A = 30$ dB.

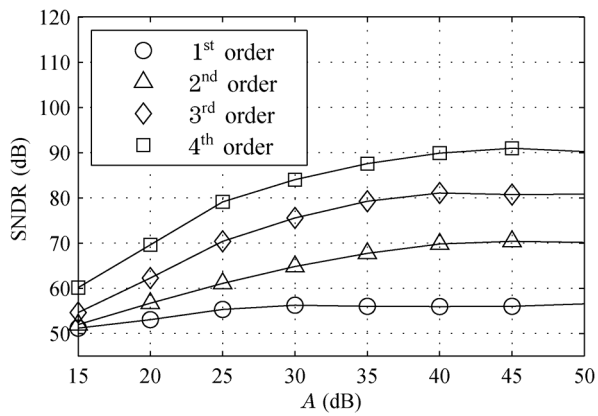


Fig. 5. SNDR versus finite opamp gain A for $\mathrm{OSR} = 70$.

fourth order, while the scaling was adjusted to keep the integrator swings below 40 mV and the coefficients were calculated under loop stability constraints.

As subthreshold operation is enforced by the low supply voltage, speed is limited and the OSR should be set as small as possible. According to the simulations in Fig. 4 the SNDR drops significantly below $\mathrm{OSR} = 70$, so that this value was adopted for a good tradeoff between speed and resolution.

Furthermore, the SNDR is circuit noise limited to about 67 dB (Section III-E), so that a second-order loop is theoretically sufficient. However, finite opamp gain can degrade the SNDR below the noise limitation (Fig. 5), so that a third-order loop (Fig. 3) was adopted to obtain more security margin to opamp gain variations.

C. Coefficients and Scaling

The noise transfer function (NTF) $H(z)$ of the modulators with order 1 to 4 in Figs. 4 and 5 was realized as a high-pass Butterworth filter with a pass-band gain of 3 dB. For the third-order modulator $H(z)$ can therefore be expressed by

$$H(z) = \frac{1}{1 + L_0(z)} = \frac{(z-1)^3}{z^3 + c_2 z^2 + c_1 z + c_0} \tag{4}$$

with $L_0(z)$ denoting the loop filter transfer function and

$$\begin{aligned} c_2 &= b_1 a_1 + b_1 b_2 a_2 - 3 \\ c_1 &= 3 - 2 b_1 a_1 - b_1 b_2 a_2 + b_1 b_2 b_3 a_3 \\ c_0 &= b_1 a_1 - 1. \end{aligned}$$

The signal transfer function (STF) $G(z)$ can be found to be

$$G(z) = \frac{a_0 + L_0(z)}{1 + L_0(z)}. \tag{5}$$

For $a_0 = 1$ the STF is exactly one while for $a_0 < 1$ low-pass behavior is present.

For the third-order modulator the resulting feedforward coefficients $a_1 - a_3$ are listed in Fig. 3 along with the scaling coefficients $b_1 - b_3$, that were chosen in a way to limit the voltage swing of all integrators to 40 mV (the maximum linear swing for $V_{\mathrm{DD}} = 250$ mV). In the same way the input coupling coefficient a_0 was adjusted to minimize the integrator voltage swings.

D. Modeling Finite Gain

The impact of finite opamp gain A was simulated depending on the modulator order (Fig. 5). Using simple inverter based integrators with intrinsic gain as low as 20 dB at a low supply

voltage, the expected SNDR is slightly above 60 dB for third order.

E. Noise and Jitter

As the input-referred noise contribution of the second and third integrator is highly suppressed by the first integrator gain, the total input-referred noise power can be approximated by considering only the first integrator noise.

The integrator noise floor has contributions both from the input sampling phase (ϕ_1) and the amplification phase (ϕ_2) (Section IV-B). During input sampling, noise is sampled on C_1 along with the input signal, giving the contribution

$$P_{\mathrm{noise}_{\phi_1}} = \frac{kT}{C_1}. \tag{6}$$

During the amplification phase another noise contribution is sampled on C_1, which is uncorrelated to $P_{\mathrm{noise}_{\phi_1}}$. Noise is also sampled on C_2, which can be referred to the input by dividing by the integrator gain C_1/C_2. A third noise contribution is added by the inverter amplifier and can be derived at the output as follows:

$$\begin{aligned} P_{\text{noise-amp}} &= \int_0^\infty V_{ni}^2(f) \cdot \frac{1}{(f/BW)^2+1} \cdot \frac{1}{\beta^2} \cdot df \\ &= V_{ni}^2 \cdot BW \cdot \frac{\pi}{2} \cdot \frac{1}{\beta^2} \end{aligned} \tag{7}$$

with the amplifier input-referred noise power spectral density (PSD) $V_{ni}^2(f)$, bandwidth BW and feedback factor β, that can be expressed as

$$V_{ni}^2 = 4kT \cdot \gamma \cdot \left(\frac{1}{g_{\mathrm{m_N}} + g_{\mathrm{m_P}}}\right) \approx 2kT \cdot \gamma \cdot \frac{1}{g_{\mathrm{m}}} \tag{8}$$

$$BW = \frac{g_{\mathrm{m_N}} + g_{\mathrm{m_P}}}{2 \cdot \pi \cdot C_{\mathrm{Leff}}} \cdot \beta \approx 2 \cdot \frac{g_{\mathrm{m}}}{2 \cdot \pi \cdot C_{\mathrm{Leff}}} \cdot \beta \tag{9}$$

$$C_{\mathrm{Leff}} = \frac{C_1 \cdot C_2}{C_1 + C_2} + C_{\mathrm{cs}} + C_1(2^{\mathrm{nd}}\mathrm{stage}) \tag{10}$$

$$\beta = \frac{C_2}{C_1 + C_2} \tag{11}$$

where the NMOS and PMOS transconductances ($g_{\mathrm{m_N}}$ and $g_{\mathrm{m_P}}$) are assumed to have the the same value g_{m} for simplicity. Moreover, according to circuit level simulations $\gamma \approx 1$. Substituting (8)–(11) into (7) yields

$$P_{\text{noise-amp}} = \frac{kT}{C_{\mathrm{Leff}}} \cdot \gamma \cdot \frac{C_2 + C_1}{C_2}. \tag{12}$$

For the first integrator $C_2 = 8 \cdot C_1$ so that (12) can be approximated by

$$P_{\text{noise-amp}} \approx \frac{kT}{C_{\mathrm{Leff}}} \cdot \gamma. \tag{13}$$

In order to compare the opamp noise to the signal it has to be referred to the signal input of the feedback network by dividing the output noise voltage by the signal gain C_1/C_2:

$$P_{i\text{noise-amp}} \approx \frac{kT}{C_{\mathrm{Leff}}} \cdot \gamma \cdot \left(\frac{C_2}{C_1}\right)^2. \tag{14}$$

Then summing up the noise contribution of both phases and adding the noise of both differential loop branches yields

$$P_{\mathrm{noise_{total}}} \approx 4 \cdot \frac{kT}{C_1} + 2 \cdot \left(\frac{C_2}{C_1}\right)^2 \cdot \frac{kT}{C_2} + 2 \cdot \frac{kT}{C_{\mathrm{Leff}}} \cdot \gamma \cdot \left(\frac{C_2}{C_1}\right)^2. \tag{15}$$

Injecting this noise power in front of the first integrator in the third-order system level simulation yields SNDR $= 67$ dB for $C_1 = 0.376$ pF, $C_2 = 3$ pF and $A = 30$ dB. Comparison to the noiseless simulations in Fig. 5 shows that the SNDR is noise limited for intrinsic gain values above 25 dB.

As for sampled systems the absolute clock period is not important as long as the variation is below a level that effects signal settling [24], clock jitter is only modeled for the input sampling process by generating an input signal of the form

$$V_{\mathrm{in}} = V_{amp} \cdot \sin\left(2\pi f \cdot (n \cdot T + t_{\mathrm{jitter}})\right) \tag{16}$$

with the sampling period T and the sample count n. The signal t_{jitter} is white Gaussian timing noise with variance σ_{jitter}. According to system level simulations the SNDR of the third-order modulator is unaffected up to a jitter variance $\sigma_{\mathrm{jitter}} = 0.166 \cdot T$. This corresponds to the analytical prediction [25]

$$\sigma_{\mathrm{jitter}} = \sqrt{\frac{\mathrm{OSR}}{(2\pi BW)^2 \cdot \mathrm{SNDR}}} \tag{17}$$

where BW denotes the bandwidth of the converter.

IV. Circuit Implementation

The small headroom available at an ultra-low voltage power supply enforces two stack transistor circuits. Therefore, in this design the integrators are implemented by inverter based-amplifiers, that reduce the amount of analog circuitry to a minimum. However, inverter based amplifiers are more vulnerable to power supply noise, so that a differential loop structure was implemented that is depicted in Fig. 6. Because of the missing tail current source only a pseudo differential design is feasible, so that additional circuitry is needed to prevent CM accumulation by the integrators. Thus, a DT CM feedback loop was provided to all integrators to reduce their CM gain to 1, thereby preventing accumulation. However, with a CM gain of one large input CM can still saturate the integrator outputs, so that CM cancellation was employed at the two input coupling nodes, the first integrator input and the comparator input. The comparator is designed to operate at ultra-low voltage by relying on two stack transistors in combination with body input techniques. The $\Delta\Sigma$ converter relies on a two phase clock, with one calibration phase to reduce offset and define process independent biasing in the analog building blocks and one active phase for voltage integration.

In this design values for $|V_{\mathrm{th}}|$ are slightly higher than V_{DD} ($V_{\mathrm{thn}} = 270$ mV, $V_{\mathrm{thp}} = -280$ mV), so that all transistors operate in weak inversion. As a convention in the following circuit diagrams all NMOS bulk connections are tied to ground and all PMOS bulk connections are tied to V_{DD} if not noted differently.

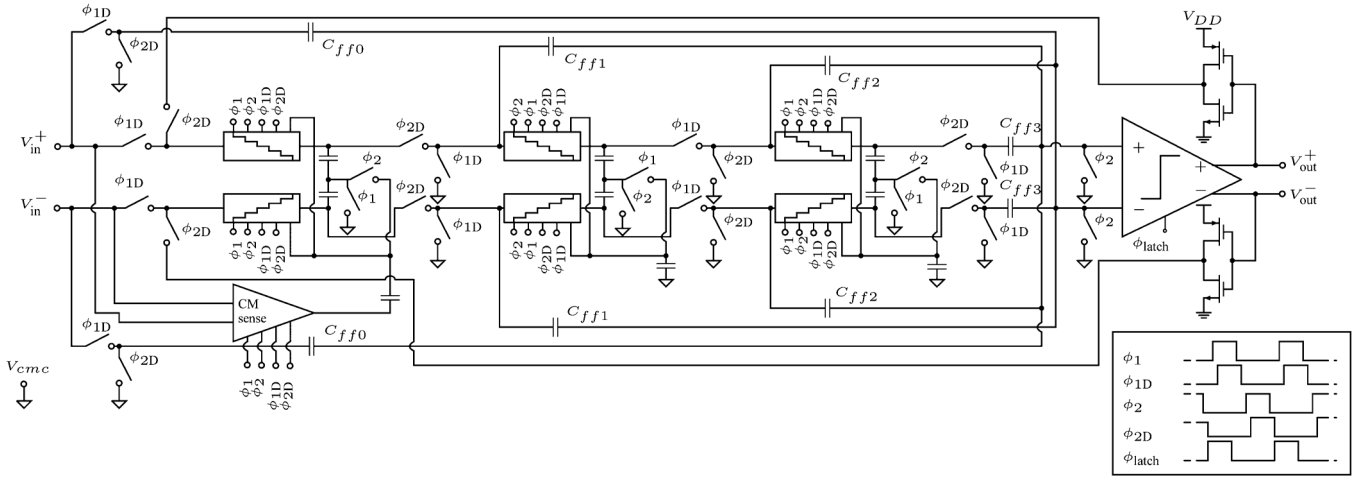


Fig. 6. Pseudo differential $\Delta\Sigma$ converter loop.

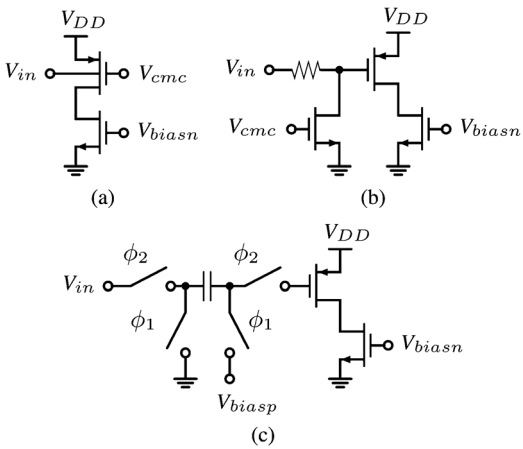


Fig. 7. Low voltage strategies for large overdrive (only half circuits shown for simplicity). (a) Bulk input. (b) Resistive level shift. (c) Capacitive level shift.

A. Amplifier Design

Since the tail current source has to be eliminated in a two stack transistor design, a major challenge is to maintain sufficient CMRR. Moreover, the CM input should be set to the supply mid-level for maximum voltage swing. However, this results in poor overdrive and consequently limited biasing current and speed. In order to realize large overdrive while decoupling the bias current from the CM input for a two transistor stack circuit, special circuit techniques are required (Fig. 7).

As for $V_{\rm DD} < 0.5$ V there is little risk in bulk forward biasing [26], a solution is using the PMOS bulk as input terminal [22] [Fig. 7(a)]. In this way the input CM can be set to the supply mid-level, while the gate can be biased close to ground. For good bias current definition, a CM control signal $(V_{\rm cmc})$ must be imposed on the PMOS gate biasing voltage while the NMOS load transistor is operated as a current source with $V_{\rm gs} = V_{\rm DD} - |\Delta V_{\rm th}|$ [13]. The term $|\Delta V_{\rm th}|$ denotes the maximum process variation in $V_{\rm th}$. Since $g_{\rm mb}/g_{\rm m} \approx 0.2$, a 250 mV rail-to-rail CM variation at the PMOS bulk input can be compensated by only 50 mV increase in CM control voltage at the PMOS gate. However, this advantage is traded against the small input transconductance $g_{\rm mb}$, resulting in low gain and GBW as well as higher input-referred noise and offset.

In another solution the input CM is level-shifted to a fixed voltage close to the supply rail via a resistor [Fig. 7(b)]. This allows the CM input to be set to the supply mid-level, while large overdrive is available for the input transistor. However, the resistor current needs to be adjusted via a CMFB loop, which will directly inject high noise levels to the input. Replacing the current source transistor by a simple resistor without feedback [22] eliminates noise amplification but input CM shift and process variation in the input transistor cannot be compensated anymore, thus making the bias current very sensitive.

Instead of level shifting the input CM via a resistor in CT, it can be capacitively shifted in DT [27], [28] [Fig. 7(c)]. A capacitor is first charged to $V_{\rm biasp}$ referred to ground (ϕ_1) and then switched in series to the gate (ϕ_2), giving only rise to kT/C noise while compensating process variation without CM feedback circuitry.

B. Integrator Design

Due to its superiority in realizing large overdrive and CM cancellation, the SC technique was applied in the integrator design of the modulator. In order to double the gain, PMOS and NMOS gates are both used as input terminals, thus resulting in an inverter based topology [1] [Fig. 8(a)]. However, in order to obtain good bias current control and larger overdrives, the NMOS and PMOS gates are capacitively biased independently [28].

The converter is a two-phase system that consists of a biasing and offset compensation phase (ϕ_1) as well as an amplification phase (ϕ_2). During ϕ_1 the CMOS inverter is biased near $V_{\rm th}$ and offset compensated simultaneously using the proposed SC biasing approach in Fig. 9(a). The biasing capacitor $C_{\rm c1}$ is charged to $V_{\rm biasn}$ referred to a CM control voltage $V_{\rm cmc}$, yielding $V_{\rm gsn} = V_{\rm biasn}$, which is set close to $V_{\rm th_n}$. In a similar fashion the biasing capacitor $C_{\rm c2}$ is charged to $V_{\rm biasp}$ referred to $V_{\rm biasn}$, yielding $V_{\rm gsp} = V_{\rm biasp} - V_{\rm DD}$, which is set close to $V_{\rm th_p}$. As both gates are biased independently, uncorrelated $V_{\rm th}$ variations in PMOS and NMOS can be compensated.

During offset compensation, the output must be fed back to the input but the PMOS gate bias is close to ground and the NMOS gate bias is close to $V_{\rm DD}$ so that neither of them can

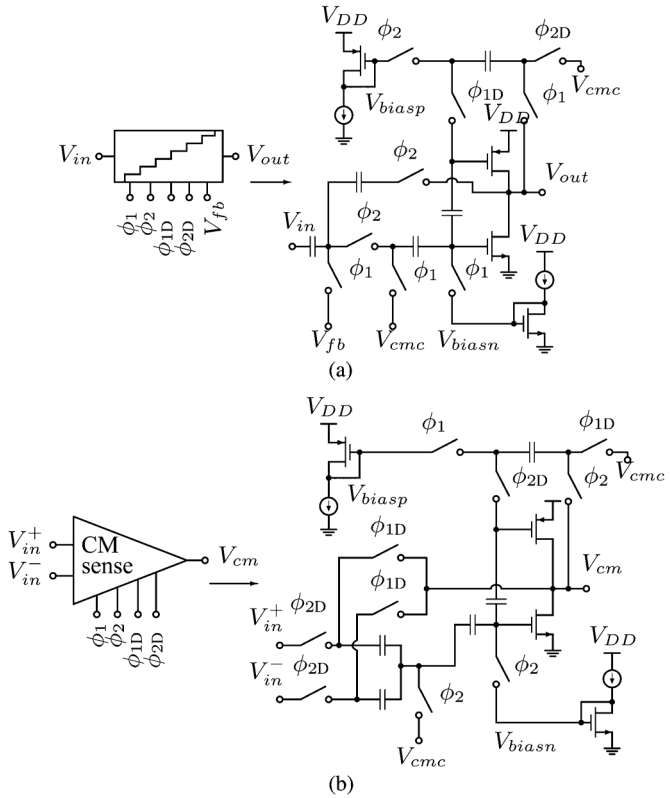


Fig. 8. Inverter based SC building blocks. (a) Biased inverter based integrator (only half-circuit shown for simplicity). (b) CM sense amplifier.

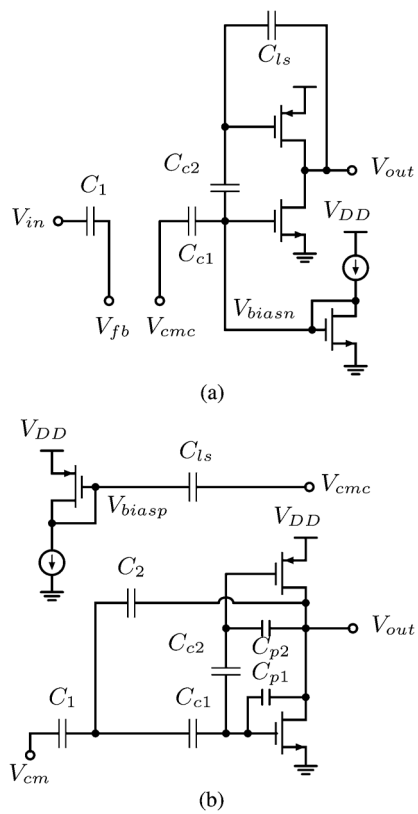


Fig. 9. Integrator clock phases (only half-circuits shown for simplicity). (a) Biasing and offset comp. phase ($\phi_1 = 1$). (b) Amplification phase ($\phi_2 = 1$).

be connected to the output directly, for this would push the inverter out of saturation. For that reason, the PMOS gate is connected to the output via level shifting capacitor $C_{\rm ls}$, that has been pre-charged to $V_{\rm cmc} - V_{\rm biasp}$ during ϕ_2. Therefore, during the biasing and offset compensation phase the inverter output settles to $V_{\rm cmc} + V_{\rm offset}$ while the PMOS gate is set to $V_{\rm biasp} + V_{\rm offset}$. As a result, C_{C2} stores both the biasing voltage for the PMOS transistor and the inverter offset.

In this way high overdrive voltage can be accomplished and the residual offset due to gain error is reduced because the output remains near $V_{\rm cmc}$ during compensation. This is one of the major key points why robust operation near $V_{\rm th}$ at 250 mV power supply is achieved.

While the inverter is biased and offset compensated, the input capacitor C_1 is charged to $V_{\rm in}$ referred to the CM feedback signal $V_{\rm fb}$. In this way the CM is cancelled before it can be seen by the inverter in phase ϕ_2.

During the amplification phase ϕ_2 the charge on C_1 is transferred to the output capacitor C_2, so that the integration can be performed on the differential mode (DM) signal. Meanwhile the level shifting capacitor is being charged to $V_{\rm biasp}$ to make it ready for ϕ_1.

For the proposed biasing scheme it is crucial that charge on the gate series capacitances $C_{\rm c1}$ and $C_{\rm c2}$ is maintained sufficiently until charge refreshing during the next clock cycle. With $C_{\rm c} = 1.2$ pF and $f_S = 1.4$ MHz a maximum leakage current of 17 nA is allowed for a maximum voltage droop of 10 mV. Charge loss is caused mainly due to subthreshold leakage current of the switches as well as gate leakage. Subthreshold leakage current of the switches at fast corner amounts to 1 nA at room temperature and reaches 12 nA at 100°C in the chosen RFCMOS technology. To see the impact of technology scaling, the predicted switch leakage currents for standard high-performance (HP) and low standby power digital technologies are presented in Table I [29]. It can be inferred from this table, that the effective switch leakage current slightly increases with scaling. Moreover, leakage current concerns can be eliminated all together by switching to a LSTP technology. Apart from subthreshold leakage gate leakage current must be considered. With standard SiO_2 gate insulators gate leakage will exceed subthreshold current considerably with decreasing oxide thickness in deeply scaled technologies. However, the use of high-k dielectrics limits the gate leakage current to below subthreshold leakage. In LSBP technologies gate leakage is even further reduced.

The CM feedback circuitry is depicted in Fig. 10(a). During ϕ_1 the integrators are in the biasing state and their output at $V_{\rm cmc}$. Therefore, the CM sampling capacitors $C_{\rm cs}$ are completely discharged, which is important to guarantee that no trapped charge creates false CM sense voltages. During ϕ_2, the integrators are in the amplification phase and their output CM is sensed by $C_{\rm cs}$ and sampled on $C_{\rm s}$. The sampled voltage on $C_{\rm s}$ is subtracted from the input during the next biasing phase, leading a total delay of one cycle [Fig. 10(b)]. The CM transfer function can therefore be written in the z domain as follows:

$$V_{\rm out_{CM}}(z) = \frac{A_1}{z-1} \cdot \left(V_{\rm in_{CM}}(z) - A_2 \cdot V_{\rm out_{CM}}\right) = \frac{A_1}{z - 1 + A_1 A_2}. \quad (18)$$

TABLE I
PREDICTED SWITCH LEAKAGE CURRENT VERSUS TECHNOLOGY NODE [29]

Technologt Node	90 nm	65 nm	45 nm	32 nm	22 nm
I_{off} (μA/μm) (HP)	0.15	0.34	0.61	0.84	0.37
I_{off} (μA/μm) (LSTP)	10^{-5}	10^{-5}	$3\cdot10^{-5}$	$3\cdot10^{-5}$	$2\cdot10^{-5}$
I_{off} switch ($\frac{W}{L}=\frac{2\cdot L_{min}}{L_{min}}$)(nA) (HP)	27	44.2	54.9	53.76	16.28
I_{off} switch ($\frac{W}{L}=\frac{2\cdot L_{min}}{L_{min}}$) (pA) (LSTP)	1.8	1.3	2.7	1.92	0.88

TABLE II
SIMULATED INVERTER AMPLIFIER PERFORMANCE VERSUS PROCESS CORNERS

V_{DD} = 250 mV												
corner	I_{bias1}	A_1	GBW_1	C_{L1}	I_{bias2}	A_2	GBW_2	C_{L2}	I_{bias3}	A_3	GBW_3	C_{L3}
slow	1 μA	31 dB	2.6 MHz		0.5 μA	31 dB	2.5 MHz		0.5 μA	31 dB	5.6 MHz	
typical	2.46 μA	30 dB	6.3 MHz	3 pF	1.23 μA	30 dB	6.2 MHz	1.54 pF	1.23 μA	30 dB	13.6 MHz	0.69 pF
fast	3.05 μA	29.6 dB	7.9 MHz		1.53 μA	29.6 dB	7.7 MHz		1.53 μA	29.6 dB	17 MHz	
V_{DD} = 300 mV												
corner	I_{bias1}	A_1	GBW_1	C_{L1}	I_{bias2}	A_2	GBW_2	C_{L2}	I_{bias3}	A_3	GBW_3	C_{L3}
slow	2.46 μA	32.4 dB	6.4 MHz		1.21 μA	32.4 dB	6.3 MHz		1.21 μA	32.4 dB	13.8 MHz	
typical	2.9 μA	32.1 dB	7.5 MHz	3 pF	1.45 μA	32.1 dB	7.3 MHz	1.54 pF	1.45 μA	32.1 dB	16.1 MHz	0.69 pF
fast	3.3 μA	31.8 dB	8.5 MHz		1.67 μA	31.8 dB	8.3 MHz		1.67 μA	31.8 dB	18.3 MHz	

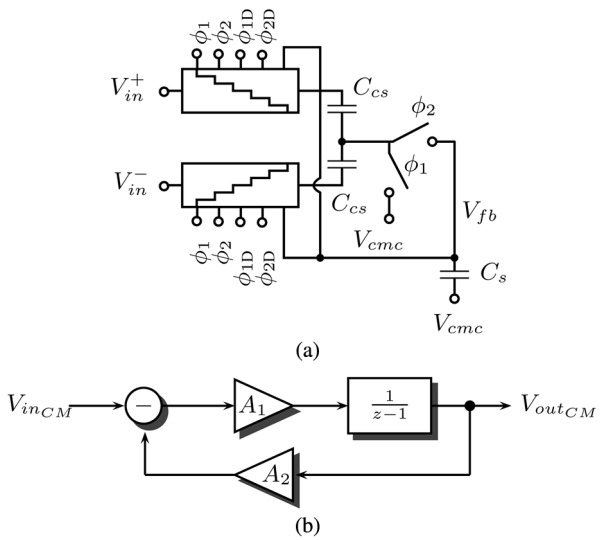


Fig. 10. CM feedback circuitry. (a) Circuit level. (b) System level.

This is stable for $A_2 < 2/A_1$. With $A_1 = C_1/C_2$ and $A_2 = C_{\rm cs}/C_{\rm cs}+C_{\rm s}$ stability is always implied for $A_1 < 1$, which is the case for the scaling coefficients listed in Fig. 3. Moreover, the settled CM output ($t=\infty$) can be found by setting $z=1$ in (18), which yields

$$V_{\rm out_{CM}}(t=\infty)=\frac{1}{A_2}. \tag{19}$$

Therefore, setting $C_{\rm cs} \gg C_{\rm s}$ reduces the integrator CM gain to about 1.

The input CM sense amplifier [Fig. 8(b)] uses the same biased inverter amplifier but with opposite clock phases, because the CM needs to be available for the integrator during the biasing phase ϕ_1. Therefore, the CM sense amplifier needs to amplify during ϕ_1. The sensed input CM is added to the CM feedback signal so that both are subtracted from the input during ϕ_1 simultaneously.

C. Integrator Performance Limitations

Limitations on gain accuracy arise from low intrinsic inverter gain (≈30 dB) and gain error caused by the gate serial capacitor $C_{\rm c}$ and the parasitic Miller capacitance $C_{\rm p}$ [Fig. 9(b)]. This effect can be explained easily by looking at the charge transfer during the amplification phase. When the integrator output changes from $V_{\rm cmc}$ to $V_{\rm out}$, the parasitic Miller capacitance $C_{\rm p}$ will be charged to $V_{\rm out}$. The same charge must flow onto $C_{\rm c}$, leading to additional voltage drop of $V_{\rm out}\cdot C_{\rm p}/C_{\rm c}$. Together with the gain error $V_{\rm out}/A$ this prevents complete discharge of C_1 and reduces the charge ΔQ transferred to C_2 as follows:

$$\begin{aligned}\Delta Q &= \frac{1}{C_1}\cdot\left(V_{\rm in}-\frac{V_{\rm out}}{A}-V_{\rm out}\cdot\frac{C_{\rm p}}{C_{\rm c}}\right)\\ &= \frac{1}{C_1}\cdot\left(V_{\rm in}-\frac{V_{\rm out}}{\frac{1}{1/A+C_{\rm p}/C_{\rm c}}}\right)=\frac{1}{C_1}\cdot\left(V_{\rm in}-\frac{V_{\rm out}}{A_{\rm eff}}\right).\end{aligned} \tag{20}$$

Therefore, the serial capacitor $C_{\rm c}$ can be considered as reducing the effective gain of the amplifier. This effect can be minimized by designing $C_{\rm c} \gg C_{\rm p}$.

Besides, the serial capacitor $C_{\rm c}$ adds an additional noise component $kT/C_{\rm c}$ during the biasing phase that has to be added to the total noise in (15).

The gain-bandwidth (GBW) is limited by the load capacitance C_L, which is the sum of $C_1\cdot C_2/(C_1+C_2)$, $C_{\rm cs}$, C_1 of the next stage and the feedforward capacitor $C_{\rm ff}$. Incomplete settling occurs if the sampling frequency $f_{\rm s}$ is close to the GBW. Due to limited current drive at ultra-low voltage operation, the only way to increase the GBW is to decrease the overall load capacitance. However, the capacitors need to be sufficiently larger than the parasitics in order to guarantee accurate matching. Therefore, there is a tradeoff between matching and settling accuracy. Table II lists the simulated performance of the three integrators for all process corners. As $f_{\rm s}$ is set to 1.4 MHz the GBW is about 5 to 10 times higher.

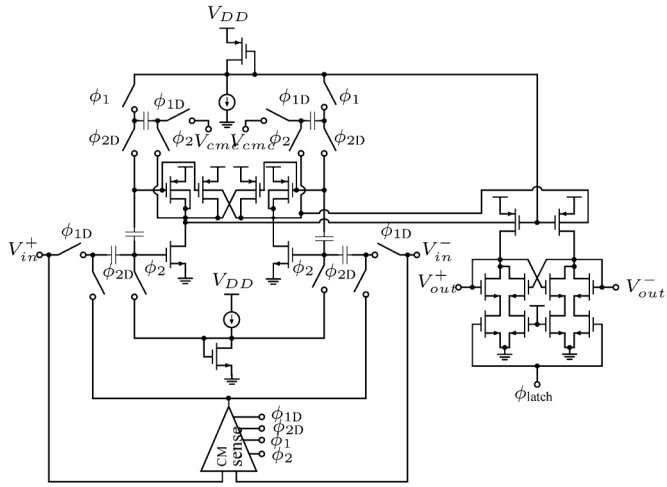


Fig. 11. Ultra-low voltage comparator.

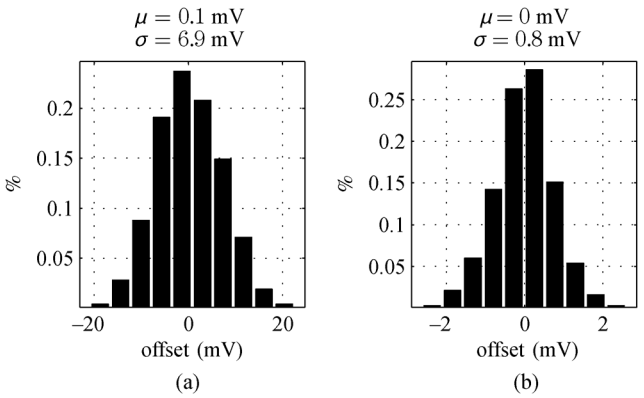


Fig. 12. Monte Carlo mismatch simulation of comparator offset (1000 runs). (a) Uncompensated. (b) Compensated.

D. Comparator Design

As the integrator swings must be highly scaled down due to limited headroom, the comparator input is small, so that a pre-amplifier is mandatory to insure proper switching of the latch. Moreover, due to the feed-forward path the comparator will see CM signals despite the cancellation in the first integrator. To meet these requirements at 250 mV power supply, an improved comparator structure was designed (Fig. 11). The CM input signals are removed by CM cancellation, so that gate input is possible which guarantees high pre-amplifier gain. Because residual CM signals might saturate the high-gain pre-amplifier, inherent CM rejection is realized by a bulk cross-coupled load that reduces the CM gain to $g_{\rm m}/g_{\rm mb} \approx 5$. The latch stage requires the load transistors to be diode-connected during the tracking phase and cross-coupled during the latch phase. Using PMOS gate input with bulk diode connection does not add enough positive feedback for successful latching because of $g_{\rm mb} < g_{\rm m}$. Therefore, the NMOS gate is diode connected, leaving only the PMOS bulk as input terminal, because the PMOS gate must be used for bias current definition. This results in an attenuation by $g_{\rm mb}/g_{\rm m}$ during the tracking phase, another reason to use a pre-amplifier.

The comparator offset is shown in the Monte Carlo simulations in Fig. 12. Without the SC offset calibration, the input-referred offset is determined by the first stage, since the second stage offset is suppressed by the pre-amplifier gain ($A = 28$ dB). The offset calibration circuitry reduces the total input-referred offset by a factor of 10. The residual offset is then mainly determined by the second stage offset divided by the pre-amplifier gain.

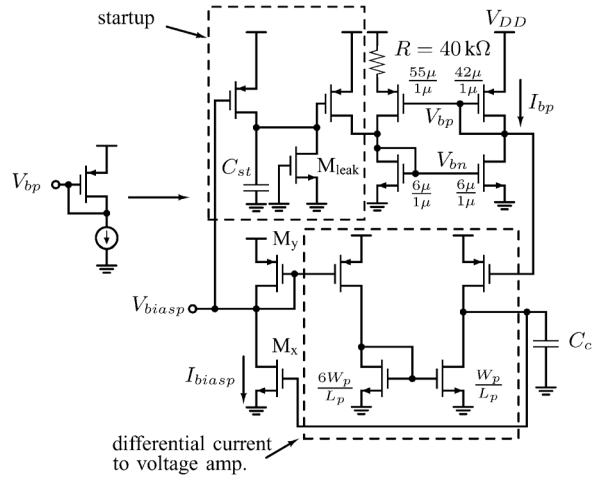


Fig. 13. Ultra-low voltage biasing circuit.

E. Biasing

Reserving headroom for a peak $V_{\rm th}$ variation of $|\Delta V_{\rm th}|$, the maximum possible biasing voltage for an NMOS and PMOS transistor is $V_{\rm DD} - |\Delta V_{\rm th}|$ and $|\Delta V_{\rm th}|$, respectively. However, this requires moving to the supply rails for slow corners, which is not feasible for a conventional constant-$g_{\rm m}$ biasing circuit due to $V_{\rm sat}$. Thus, the maximum bias voltages in a conventional constant $g_{\rm m}$ circuit are limited to

$$V_{\rm biasn} < V_{\rm DD} - V_{\rm sat} - |\Delta V_{\rm th}| \quad (21)$$

$$V_{\rm biasp} > V_{\rm sat} + |\Delta V_{\rm th}|. \quad (22)$$

This results in very small overdrives and limits the bias current to the nA range. Although current can be raised by increasing the transistor widths, this would come at the expense of significantly larger parasitic capacitances. Therefore, in combination with a low current constant $g_{\rm m}$ mirror a level-shifting circuit was designed (Fig. 13), that shifts the constant-$g_{\rm m}$ bias by 90 mV via pushing transistor M_x into triode region in a feedback configuration. This allows to reduce the inverter amplifier transistor widths by a factor 10, so that the transition frequencies for PMOS and NMOS are increased from 48 MHz to 424 MHz and 159 MHz to 760 MHz, respectively. The bias current generation is a two step process (Fig. 14), where in the first step a low current (250 nA) is generated, which is defined by the external biasing resistor R. All measurements in Section V have been performed with $R = 40$ kΩ which results in 250 nA as predicted in simulation. Due to the low bias current transistors can operate in deep subthreshold, so that the constant $g_{\rm m}$ circuit can operate at 250 mV while still reserving enough headroom for process variations. In the second step the constant $g_{\rm m}$ current is mirrored into a differential current to voltage amplifier, that compares 6 times the constant $g_{\rm m}$ current to the output bias

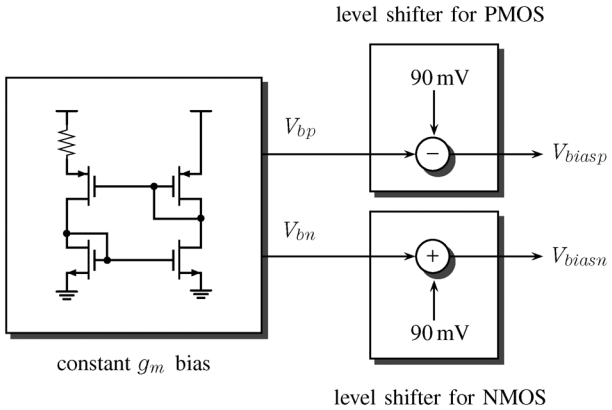


Fig. 14. Block diagram of the biasing strategy. The outputs of a low current constant $g_{\rm m}$ bias are level shifted.

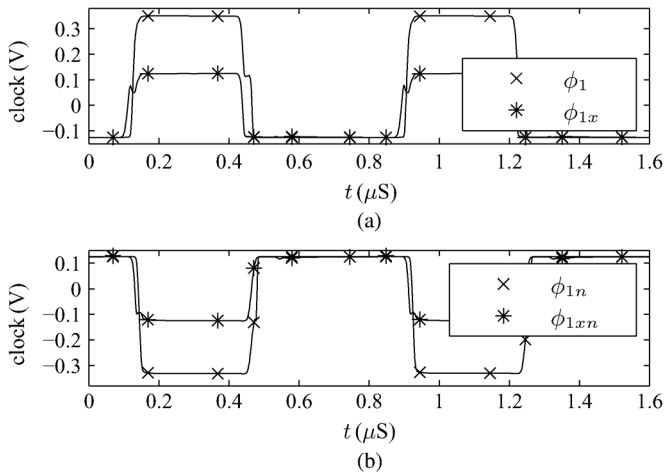


Fig. 15. Transient simulation of clock generation. (a) Clock signal for NMOS switches. (b) Clock signal for PMOS switches.

current $I_{\rm biasp}$, which is defined by $V_{\rm GS}$ over M_y. The gain of the differential current to voltage amplifier will then make sure that $I_{\rm biasp} = 6 \cdot I_{\rm bp}$. For $V_{\rm DD} = 250$ mV M_y can only conduct $I_{\rm biasp}$ by pushing M_x into triode region, which is possible due to the gain of the feedback loop. Consequently, $V_{\rm sat}$ in (22) is removed, so that $V_{\rm biasp}$ can be set to $|\Delta V_{\rm th}|$, thus increasing the transistor overdrives significantly. In the same way a level shifter was designed to generate $V_{\rm biasn}$ at $V_{\rm DD} - |\Delta V_{\rm th}|$.

For the constant $g_{\rm m}$ circuit a dynamic start-up was added to avoid the zero current state. A dynamic start-up is preferred here, because the voltage on $C_{\rm st}$ can truly track $V_{\rm DD}$, so that the start-up circuitry keeps deactivated over a wide supply range after start-up. Transistor $M_{\rm leak}$ implements a leakage current path to guarantee that trapped charge on $C_{\rm st}$ is removed before start-up.

F. Clock Generation

In order to open and close the MOS switches properly large overdrive is required. For the switches in the $\Delta\Sigma$ converter that operate near $V_{\rm cmc}$ (supply mid-level) a maximum overdrive of only 125 mV is available, which is far too low for fast switching transients. Therefore, the switches were implemented as transmission gates and driven by a clock booster [Fig. 16(b)], that doubles the clock level (Fig. 15) while all other active building blocks of the converter operate at 250 mV power supply.

In general, implementing charge pumps with good efficiency at a ultra-low supply voltage is a challenging task due to small overdrive and large reverse leakage current caused by the small difference between on and off voltage of the charge pump switches. However, boosting just the clock signal is straight forward, because the clock doubler only needs to drive the small gate capacitances of the MOS switches, so that the average load current is very low. Moreover, the clock booster in Fig. 16(b) is capable of low voltage operation, because the switch connecting the pumping capacitor to the supply is driven by the pumped output voltage [30].

The voltage boosters are preceded by a non-overlapping clock generator [Fig. 16(a)], that provides the clock timing required by the data converter. In a similar way as for the NMOS switches, a clock controller and booster was implemented for the PMOS switches.

V. Implementation and Measurement Results

The converter was implemented in 0.13 μm standard CMOS (Fig. 17) with design variables listed in Table IV, that implement the system level coefficients from Fig. 3. The parasitic Miller capacitances $C_{\rm p1}$ and $C_{\rm p2}$ are in the order of a few fF, so that according to (20) the serial capacitor $C_{\rm c}$ must be in the pF range in order not to degrade $A_{\rm eff}$. Under practical area constraints $C_{\rm c}$ cannot be set arbitrarily high, so that there is a limitation on the inverter sizing, that dictates the maximum current and the GBW. Limitations on the clock speed come from the voltage boosters, since higher speed will increase their current load by the parasitic switch capacitances. Moreover, at higher speed the clock booster capacitances are incompletely charged.

In an independent energy harvesting system the CM control voltage $V_{\rm cmc}$ can be derived by a resistive divider passively from the power supply. This has been verified with two external 100 kΩ resistors without any SNDR degradation.

Measurements have been performed on seven dies, that all perform consistently (Table V). For 250 mV power supply the converter can run up to a clock speed of 1.4 MHz, which yields 61 dB SNDR in 10 kHz bandwidth (Fig. 18). The zero input SNDR measurement in Fig. 19 shows that no tones are present in the signal band. Rising the supply to 300 mV yields more efficient voltage boosting and the maximum clock speed can be increased to 2.8 MHz, so that the bandwidth is doubled. The performance is independent on the CM as suggested by the dynamic range measurements in Fig. 20, that were performed both in fully differential and in single-ended mode. The SNDR in single-ended mode is not degraded despite the large CM voltage superimposed. This is achieved by the CM feedback and cancellation circuitry, so that the converter can handle rail to rail CM input. At $V_{\rm DD} = 250$ mV the complete $\Delta\Sigma$ converter system consumes a total power of 7.5 μW, which gives a figure of merit (FOM) of 0.41 pJ/conversion. This is compared to other works in Table III and defined as

$$\text{FOM} = \frac{P}{2^{(\text{SNDR}-1.76)/6.02} \cdot 2 \cdot BW}. \tag{23}$$

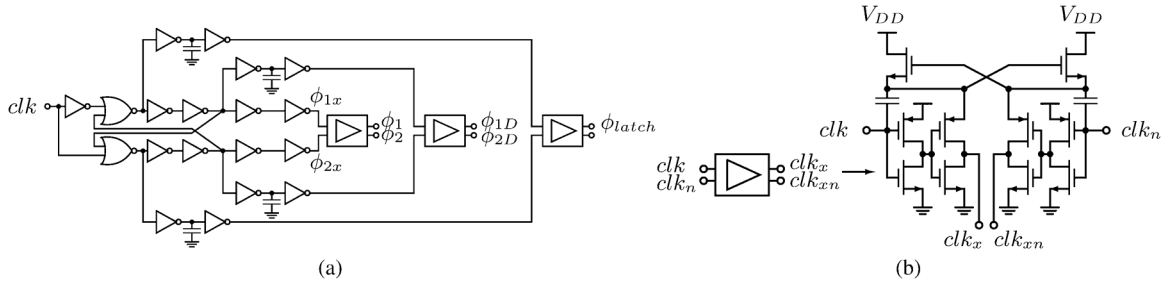


Fig. 16. Clock generation. (a) Clock controller for NMOS switches. (b) Clock booster for NMOS switches.

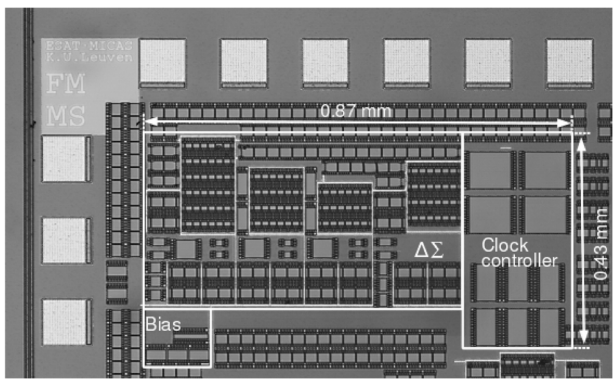


Fig. 17. Chip micrograph.

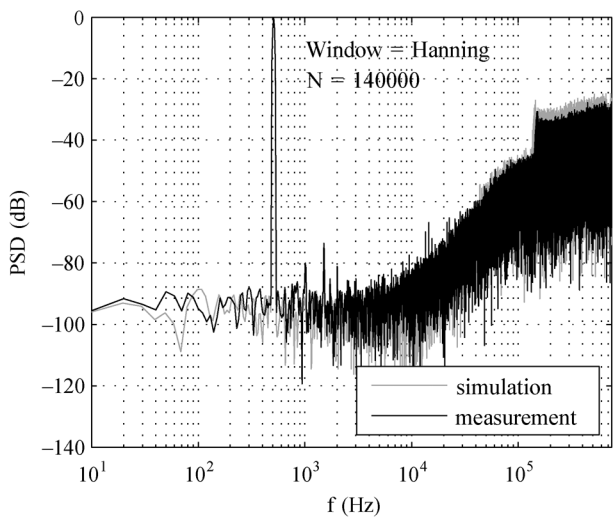


Fig. 18. Measured power spectral density for a 500 Hz sinusoidal input with 200 $\mathrm{mV_{pp}}$ at $V_{\mathrm{DD}} = 250$ mV.

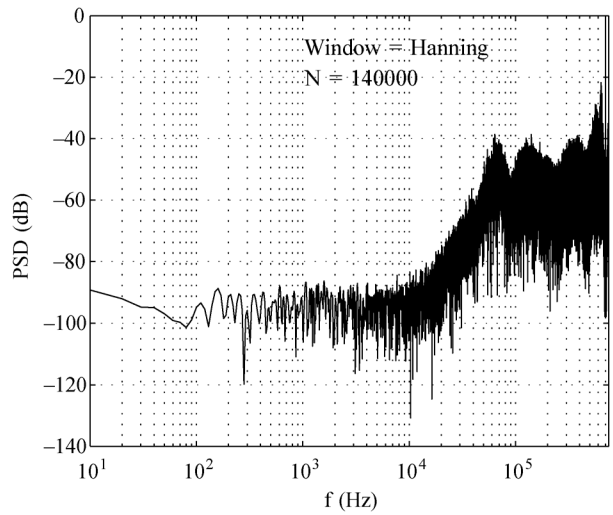


Fig. 19. Measured power spectral density with inputs shorted.

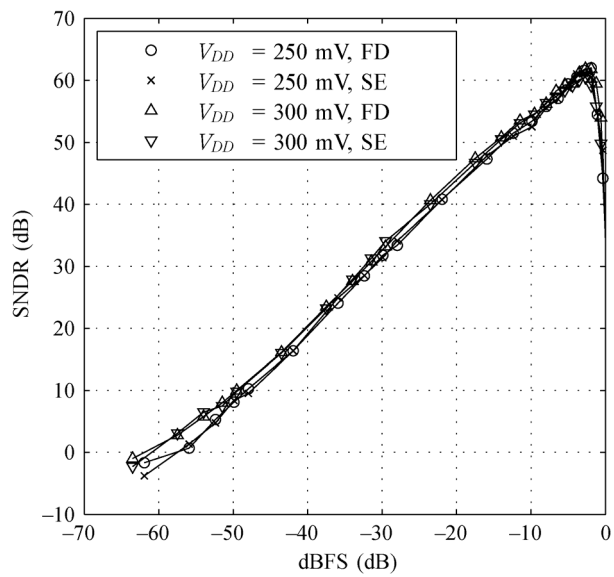


Fig. 20. SNDR versus normalized input level for a 500 Hz sinusoidal input.

Although the FOM is lowest among the converters operating below 0.6 V, on-chip biasing, clock boosting and CM feedback circuitry cause additional overhead, that is required for robust operation at 250 mV. Moreover, small signal swings degrade the SNDR, so that the FOM is worse compared to the 0.6 V [20], 0.65 V [31] and 0.7 V [1] designs. This confirms an important fact, that there is a supply voltage optimum around 0.6 V. However, the optimum supply point cannot always be chosen, because scaling of digital blocks continues and many low voltage applications [12]–[14], [16] enforce operation below the optimum supply voltage. For these application enabling functionality is more important than optimum FOM.

For typical and fast process corners, the converter can operate with a power supply of only 250 mV, whereas for a power supply of 300 mV all process corners can be covered. For this reason the temperature range (Fig. 21) is extended to lower temperatures for higher supply voltages, which is equivalent to approaching the slow corner. Therefore, there is a clear tradeoff between supply voltage and lower temperature range. If for some ap-

TABLE III
COMPARISON TO OTHER WORKS

	type	V_{DD} [V]	$SNDR$ [dB]	BW [kHz]	P [μW]	Area [mm^2]	CM input range	Temp. range [°C]	technology	V_{thn} [V] V_{thp} [V]	FOM [pJ/step]
This work, 2011	DT	0.25	61	10	7.5	0.3375	rail to rail	20-100	0.13 μm standard CMOS	0.27 -0.28	0.41
This work, 2011	DT	0.3	61.4	20	18.3	0.3375	rail to rail	0-100	0.13 μm standard CMOS	0.27 -0.28	0.477
Ishida, 2005 [19]	DT	0.5	39.6	8	75	0.025	-	-	0.15 μm SOI	0.1 -0.1	60.1
Pun, 2007 [21]	CT	0.5	74	25	300	0.6	-	25-105	0.18 μm tripple well	0.5 -0.5	1.46
Chen, 2011 [17]	CT	0.5	81.2	25	625	0.8	-	0-70	0.13 μm tripple well	0.28 -0.26	1.33
Sauerbrey, 2006 [32]	DT	0.6 (0.5)	65 (62)	312	7200 (6500)	2.2	-	-	90 nm standard CMOS	-	7.94
Ahn, 2005 [18]	DT	0.6	81	20	1000	2.9	-	-	0.35 μm standard CMOS	0.34 -0.31	2.73
Roh, 2009 [20]	DT	0.6	81	20	34	0.33	-	-	0.13 μm standard CMOS	0.2 -0.15	0.093
Gambini, 2007 [31]	DT	0.65	59.5	50	27	0.11	-	-	90 nm standard CMOS	-	0.35
Chae, 2008 [1]	DT	0.7	81	20	36	0.715	-	-	0.18 μm standard CMOS	-	0.098
Sauerbrey, 2002 [33]	DT	0.7	67	8	80	0.082	-	-	0.18 μm standard CMOS	0.43 -0.38	2.733

TABLE IV
DESIGN VALUES

	W_n/L_n	W_p/L_p	C_1	C_2	C_{cn}	C_{cp}	C_{cs}	C_s	C_{ff}
Integrator 1	6 μm/0.5 μm	20 μm/0.25 μm	0.38 pF	3 pF	1.2 pF	1.2 pF	0.22 pF	1.7 pF	1.3 pF
Integrator 2	3 μm/0.5 μm	10 μm/0.25 μm	1.1 pF	1.1 pF	1.2 pF	1.2 pF	0.22 pF	1.7 pF	0.38 pF
Integrator 3	3 μm/0.5 μm	10 μm/0.25 μm	0.38 pF	1.1 pF	1.2 pF	1.2 pF	0.22 pF	1.7 pF	0.19 pF

TABLE V
PERFORMANCE SUMMARY

Supply Voltage ($V_{DD} - V_{SS}$)	**250 mV**	**300 mV**
Technology	standard CMOS 0.13 μm twin well	
Threshold voltage	V_{t_n} = 270 mV, V_{t_p} = -280 mV	
DM Input range	200 mV	240 mV
CM Input range	rail to rail	
Total Power consumption	7.5 μW	18.3 μW
Power consumption analog	4.825 μW	9.36 μW
Power consumption digital	2.675 μW	8.94 μW
CMRR	49 dB @ 5 kHz, 100 mV_{pp}	49 dB @ 10 kHz, 100 mV_{pp}
PSRR	34 dB @ 5 kHz, 15 mV_{pp}	44 dB @ 10 kHz, 50 mV_{pp}
Sampling Frequency	1.4 MHz	2.8 MHz
Bandwidth	10 kHz	20 kHz
OSR	70	70
Peak SNDR	61 dB	61.4 dB
Peak SFDR	70 dB	66 dB
Peak SNR	64 dB	70 dB
Die Area	0.3375 mm^2	
Temperature Range	20 - 100 °C	0 - 100 °C

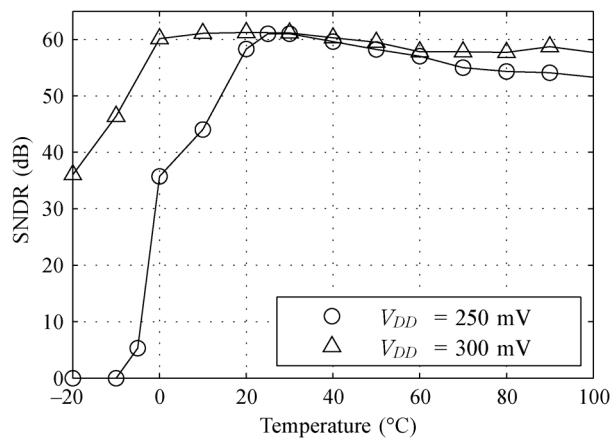


Fig. 21. SNDR versus temperature for a 500 Hz sinusoidal input.

plications negative temperature range is required, the supply voltage would have to be increased beyond 300 mV.

Apart from achieving constant SNDR over temperature variation, the supply susceptibility is well controlled (Fig. 22 and Fig. 23). The converter can work up to 0.6 V power supply, while keeping the increase in analog current consumption low. Robustness to PVT is accomplished by the on-chip biasing circuit, that can compensate for $V_{\rm th}$ shifts while still realizing overdrives close to the supply rails.

VI. CONCLUSION

An ultra-low voltage $\Delta\Sigma$ converter was designed using a SC biasing technique, that enables PVT independent biasing of inverter based integrators. Moreover, an on-chip biasing circuit was proposed, that can overcome the limitation of $V_{\rm sat}$ in the conventional constant $g_{\rm m}$ circuit, thereby increasing the maximum possible overdrive significantly. With an OSR of 70 61 dB SNDR in 10 kHz BW for a differential mode input signal of 200 mV_{pp} is achieved at a supply voltage of only 250 mV. Raising the power supply to 300 mV allows to increase the temperature range and bandwidth. Furthermore, the circuit achieves the performance up to 600 mV power supply. As a result the complete converter can operate under PVT variation at 250 mV (the lowest reported value for $\Delta\Sigma$ in bulk CMOS) by coping

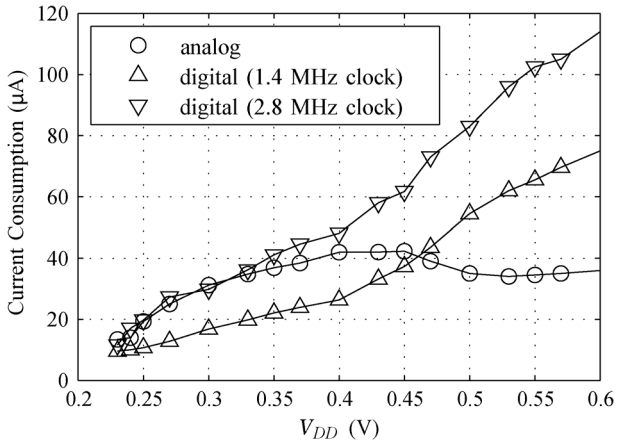


Fig. 22. Analog and digital supply current versus supply voltage.

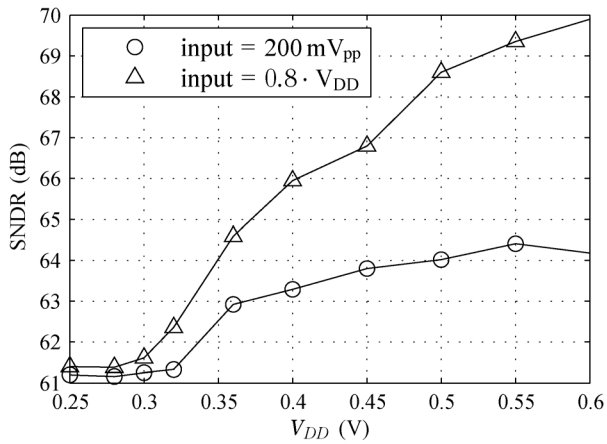


Fig. 23. SNDR versus supply voltage.

with limited voltage headroom owing to the developed near-threshold-voltage biasing technique.

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